Applied GIS

ISSN: 1832-5505

Vol-10 Issue-04 OCT 2022

Quantum dot cellular automata with a reversible ALU: a novel design and simulation

R SRAVANTHI[1], M GIRIBABU[2]

Assistant professor[1,2]

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

P.B.R. VISVODAYA INSTITUTE OF TECHNOLOGY & SCIENCE S.P.S. R NELLORE DIST, A.P, INDIA, KAVALI-524201

Abstract

Due to its tiny size, fast latency, and very low power consumption, quantum dot cellular automata (QCA) technology can help alleviate problems with the construction of nanoscale CMOS-based digital circuits. The ALU is the "brain" of a contemporary central processing unit (CPU). This paper uses quantitative circuit analysis (QCA) to detail how to assemble a reversible ALU unit using both conventional reversible blocks and a novel reversible block design, the BS1 Block. In the proposed method, the block performs all computations and assessments. The proposed architecture can be evaluated for viability using QCA Builder. Modelling results indicate that the proposed layout beats its predecessors in three critical areas: reducing the quantum cost by 30%, expanding the number of cells by 27%, and by 30%. (Requires a smaller actual footprint).

Keywords: Quantum dot cellular automata (QCA) · Reversible logic · Arithmetic logic unit (ALU) · QCA designer.

Introduction

The major challenges to the advancement of digital circuitry in systems are energy loss and excessive power usage [1]. Power usage will skyrocket if nanotechnology implementations of irrevocable circuitry are made. One way to lower the threshold for developing new circuits is using reversible processing [1]. Loss of knowledge results in the loss of energy. There will not be any wasted power if no data is deleted. Each bit's energy loss rate is roughly KTLn2, where K is Boltzmann's constant, T is the operating temperature in Kelvin, and n is the number of bits [2]. This was proven by Landauer in 1961. According to Moore's Law [3,] the number of transistors on silicon processors increases approximately every 18 months. Bennett demonstrated in 1973 that the energy loss in such circuits could be greatly reduced or even removed through the use of bidirectional gates [4]. Bits of data are not deleted and energy is conserved during reversible computations. Reversible logic gates are required when designing reversible circuitry. Reversible gates are logic gates with a 1:1 correspondence between their inputs and their outputs. The creation and design of circuitry for electrical devices rely heavily on CMOS technology. Due to physical limitations, CMOS technology makes it nearly difficult to design small-scale circuitry. As a result of the issues with CMOS

technology, various alternatives have been suggested. When it comes to creating digital circuitry at the nanoscale, QCA technology is one of the most effective options because it does not rely on transistors. Circuits with very small size, fast speed, and minimal power usage are all within reach with this technology. The quadrilateral corner array (QCA cell) is the fundamental building block of QCA technology. Each of the cellular foci receives a couple of electrons. The system relies on the properties of Coulombic forces. Transferring the location of electrons from one cell to another is how QCA turns cells on and off. The NOT and three input majority gates are used in QCA [5]. Sousa [6] emphasizes the significance of processing to a computer's efficiency. Several novel computational models are also being debated and examined, as are cutting-edge technologies like nanotechnology and quantum-based computing. Reversible sequence and combinational circuits have been the subject of numerous suggested and built reversible logic gates in recent years [7]. In QCA, Das et al. [8] suggested and developed a bidirectional incremented circuit. Using the Peres reversible gate, they developed a novel reversible half-adder circuit as well. Tobuild an encoder circuit using QCA technology, Das et al. [9] suggested a novel structure built on Feynman and Toffoli gates. The arithmetic logic unit (ALU) is the central processor unit's (CPU's) primary building component. Many experiments using QCA-based reversible ALUs have been suggested and developed in recent years. As an illustration, Sasami et al. [10] created a powerful bidirectional ALU unit in QCA. RUG is the building component

ISSN: 1832-5505

Vol-10 Issue-04 OCT 2022

of their suggested design. A reversible ALU unit using QCA technology is suggested in this article, along with a forty-four reversible block dubbed the BS1 Block. Feynman gates, Fredkin gates, and the suggested block are all reversible and are used in the proposed ALU design. The suggested system can execute a wide variety of mathematical and logical processes, including addition, increase, subtraction, and transfer, as well as OR, AND, and XOR. QCA technology allows for improvements in the suggested design over earlier studies, most notably in terms of reduced delay and footprint. Codesigned 2.0.3 is used to run simulations of the suggested layout [11]. In terms of quantum cost, number of cells, and number of processes, it also performs better than previous versions. In conclusion, this article makes the following contributions:

- Proposing a new reversible block that is called BS1 Block
- Design of proposed block quantum structure
- Simulate the proposed block using QCADesigner 2.0.3 tool
- Proposing a new reversible ALU
- Design of a reversible ALU unit using two gates Feynman, Fredkin and the proposed block
- Simulation of the proposed ALU using the QCADesigner 2.0.3 tool
- Calculation of evaluation parameters of the proposed structure such as number of constant inputs, number of garbage outputs, latency, quantum cost and comparison with recent research

The remaining sections of this document are structured as follows: Basic ideas of QCA technology are discussed in Section 2, including the QCA cell, wire construction, reversible logic, and the implementation of reversible gates. Somen relevant readings are discussed in Section 3. In Section 4, we examine the suggested architecture and the movable block. The modelling of the suggested architecture is described in Section 5, along with a comparison to related studies. The findings are presented in Section 6, the very last section.

Basic QCA technology concepts

The key concepts of Quantum Computer Architecture (QCA) are introduced here, including the QCA cell, wire structure, timing idea, reversible logic, and the Feynman and Fredkin reversible gates used in the suggested ALU circuit. Figures of worth are also described, including cell count, steady intake, trash output, filled area, and quantum cost.

QCA cells

Each QCA cell in QCA technology consists of 4 holes and 2 additional electrons; these electrons are allowed to travel between the holes. Two electrons can be placed in four holes in six distinct ways, but not all of these states are permanent due to the Coulomb Effect. Cell polarization is a stable condition that happens when electrons are situated at the farthest distance, or at perpendicular spots. These are the Plus 1 and 1 phases depicted in Fig. 1, which correspond to the logic 1 and logic 0 [8, 11, 12].

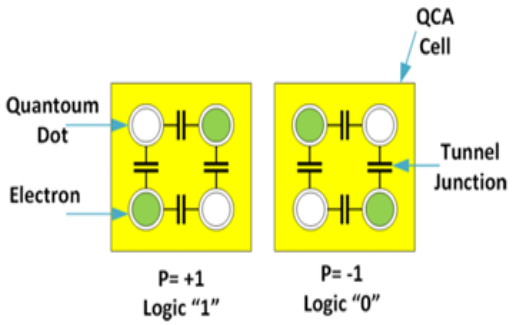


Fig. 1 Display of two stable states of the stem cell in QCA (left hand with logic 1 and right hand with logic zero) [12] .

Wire structure:

Each cell has an effect on the cells around it due to the negative force of Coulomb contact between electrons. However, when two cells are adjacent to one another, they are always oriented in such a manner as to reduce this repelling force. The QCA cells in a matrix can function as a cable to carry signals. Fig. 2 depicts two distinct types of QCA lines. In Fig. 2a, the number in the first cell is logical, and this value propagates to the other cells. A quantum wire whose cell value is the opposite of the preceding cell's structure is depicted in Figure 2b. There is a 45-degree turn in the rooms. The units in the second form, the "complement chain," are flipped by 45 degrees. Input signals travel from cell to cell and from pair to pair. These two wire models can be stacked on top of one another to create a more realistic representation of a wire.

ISSN: 1832-5505

Vol-10 Issue-04 OCT 2022

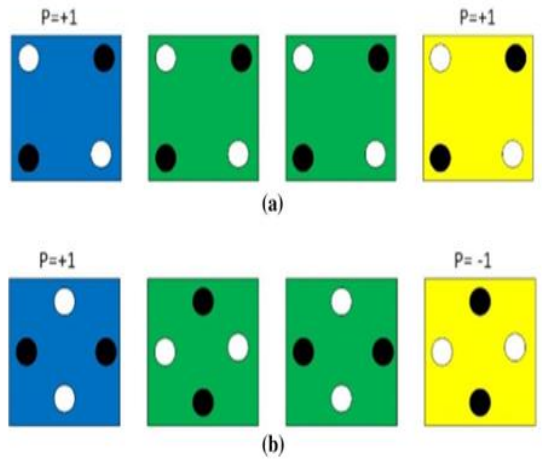
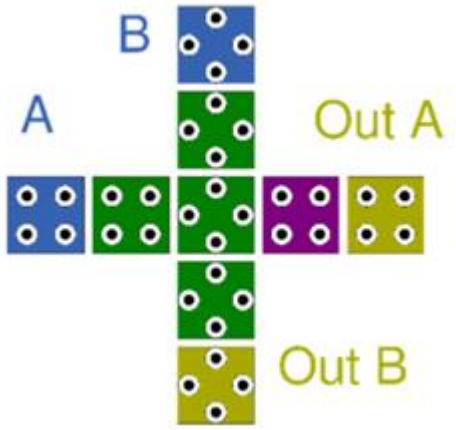


Fig. 2 a QCA standard wire; b QCA complement wire [13]

Fig. 3 Passed crossing wire model [12]



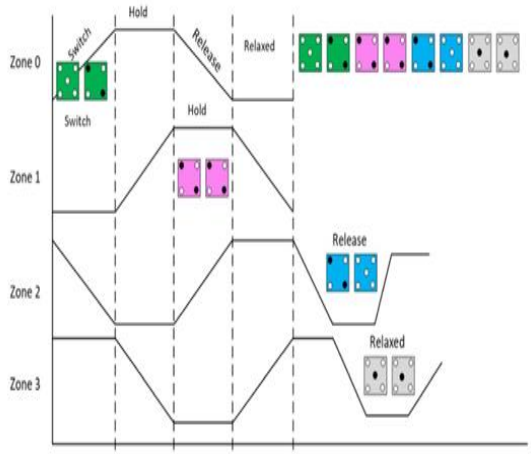


Fig. 4 Different clocking areas in QCA [17]crossing wire, which is depicted in Fig. 3. In the crossing wire model, due to the difference in cell polarity, the two wires have no effect on each other [8, 11, 12, 14, 15].

Clocking in QCA:

QCA-based circuitry employs clocking to enhance their tenable nature. In its default configuration, QCA's numerical processes are conducted in four stages, each of which is governed by a one-dimensional schedule. Each QCA circuit, as depicted in Fig. 4, consists of four timing zones, or stages, labelled Switch, Hold, Release, and Rest. These four stages are all separated from one another by 90 degrees. Electrons at the points can be influenced by neighbouring cells that are also in the switch or hold phase, and the energy limits within the point steadily grow during this phase. As the barrier force between the spots decreases in the release phase, the electrons are no longer protected from the electrons in neighbouring cells during the hold phase.

Fig. 5 Quantum structure of Feynman gate [18]

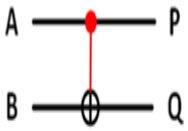
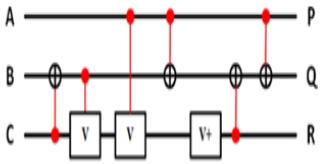


Fig. 6 Quantum structure of Fredkin gate [19]



can lessen, electrons progressively liberate, and electron movement within the cell becomes fully loose at some point [16].

Reversible logic

A bidirectional logic function is one where the output values can be used as inputs to produce the other inputs independently. It is possible to implement a bidirectional logic function with a reversible gate. The inputs and outputs of a reversible gate are both identical in quantity, and the input and output vectors are directly proportional to one another. The suggested ALU circuit's two bidirectional Feynman and Fredkin gates have their quantum structure described in Parts 2.4.1 and 2.4.2..

Feynman gate

The Feynman gate [18] is a two-input, two-output bidirectional logic gate. In Fig. 5 we see the quantum structure of this gate. P = A, Q = AB describes the Feynman gate, which takes in two inputs (A and B) and produces two outputs (P and Q). This gate has a one for its quantum cost. This gate is used to generate spread out or eliminate the restriction that arises when designing bidirectional

ISSN: 1832-5505

Vol-10 Issue-04 OCT 2022

circuits, wherein an output can only be used to one of the other inputs of the circuit gates. It is also possible to use this gate to make an input that is a counterpart of another.

Fredkin gate

The bidirectional Fredkin gate takes in and sends out three signals. The quantum cost of this obstruction is Figure 6 shows the quantum representation of this barrier. There are three inputs (labelled A, B, and C) and three outputs (labelled P, Q, and R) on this particular Fredkin gate. These findings can be explained by the equations P = A, Q = ABAC, and R = ACAB. This gate can switch the sequence of inputs B and C as a 2 to 1 multiplexer, based on the value of input A. This structure holds if (A=0), (Q=B), (R=C), and (A=1), (Q=C), and (R=B) [19].

Figures of merit

Figures of merit are quantifiable metrics used to compare the effectiveness of one approach to others. Most scholars in the field of based reversible logic systems use criteria to gauge the efficacy of their suggested technique. This essay considers the following factors:

- Constant inputs: Inputs that need to be placed in a reversible circuit with a constant zero or one.
- Garbage output: Outputs that in the reversible circuit are not considered as the main circuit output.
- Occupied area: The required space to design and simulate a circuit based on QCA technology.
- Number of cells: The number of QCA cells used to simulate a reversible circuit.
- Quantum cost: The quantum cost of each circuit depends on the 1×1 and 2×2 reversible base gates required to design it.

Related works

Chandra et al. [20] proposed a gadget that can carry out seven logical operations and eight number operations using the HNG bidirectional gate [21]. Many aspects of the architecture have been fine-tuned, including the quantum cost, the number of continuous inputs, the number of garbage outputs, the number of bidirectional gates, and the latency. Goswami et al. [22] proposed a three-layer ALU design with four thoroughly verified adder gates. It has a two-hour lag time, takes up 2.34 square meters, and has 1069 individual cells. The excessive need for space is the primary disadvantage of this design. A QCA-based single-bit ALU that includes AND, OR, XOR, and a full adder was proposed by Qadim et al. [23]. The 0.78-square-meter, 3-layer structure had a 3-second latency time and comprised 464 cells. This building project is permanent. The innovative reversible gate NHG was proposed by Alizadeh et al. [24] as part of a reversible ALU design. Their method was more involved than others, but it cut down on the resources necessary to build a similar wall. The design takes up 0.921 m2, employs 670 cells, and has a 4-cycle delay. The system can conduct 16 arithmetic and logical operations with a constant input and two waste products as outputs. Sen et al. [25] created a reversible ALU unit with testability by utilizing a reversible multiplexer. The reversible arithmetic unit (RAU) in the ALU unit is distinct from the reversible logic unit (RLU) (RLU). These components are shown separately, but the proposed ALU unit's QCA architecture is not presented. This plan uses rotating cells on a single layer, with 9 stable inputs and 15 random outputs. This design is capable of 17 distinct arithmetic and reasoning operations. In the QCA, Chavez et al. [26] presented a single-bit ALU built from four Fredkin gates and two Toffoli gates. The idea is realized with a four-way garbage can junction. There are only six possible rational operations on this platform. Sokoori et al. [27] built an ALU using a bidirectional gate called the Double Feynman gate, the AND gate.The multiplexer selects between OR and full adder outputs. Norouzi et al. [28] proposed a reversible ALU unit based on QCA technology, which uses reversible Fredkin and HNG gates. The blueprint calls for three Fredkin Gates and one HNG Gate. In the proposed setup, garbage is always emptied in the same place. The gadget is capable of performing twenty different arithmetic and reasoning operations. This setup has been modelled with 480 pieces and 0.75 m2 of surface area.

Proposed reversible ALU.

The ALU is the central working unit of any digital CPU and is crucial to the operation of the computer at all times. High power usage was the consequence of data loss in ALUs developed using irrevocable logic. Preventing the loss of such electricity is an absolute necessity for such layouts. The ALU unit's power economy can be enhanced by designing it in both directions. In this part, we'll take a closer look at the proposed reversible BS1 Block, the proposed reversible ALU design, the table of logic and math operations that can be done by the proposed design, block emulation, and the proposed design.

Proposed reversible BS1 Block

Applied GIS

ISSN: 1832-5505

Vol-10 Issue-04 OCT 2022

Four inputs (W, X, Y, and Z) and four outputs (P, Q, R, and S) make up the suggested bidirectional BS1 Block. The results can be modelled using the formulas P =M(X, Z) W, Q=Y, R =X Y Z, and S =Z. Figure 7 depicts the quantum structure of the suggested building component. This unit executes logical operations like AND, OR, XOR, and NAND in addition to arithmetic operations like addition and subtraction. This block performs as a complete adder if the input W is zero; in this instance, the result at output R is the total of the three input values X, Y, and Z, while the result at output P is the carry number. For this region, the quantum cost is a whopping six. In a nutshell, this building component offers the following benefitsThe majority of Logical operations are built inThe logic layout consists of just one majority of three inputs and two XOR gates. As a standalone device, it functions as a bidirectional complete adder.

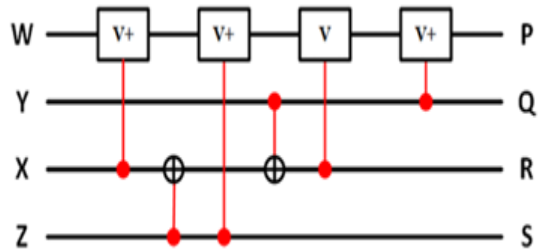


Fig. 7 The quantum structure of the proposed reversible BS1 Block

- It needs only 0.75 clock cycle to perform the operations.
- It produces only two garbage outputs.
- Its quantum cost is 6.
- Simplicity of simulating and implementing the proposed reversible block in comparison to exiting 4*4 blocks.
- Reduce the number of cells in the proposed reversible block in comparison to exiting 4*4 blocks.
- Reduce the occupied area of the proposed reversible block in comparison to exiting 4*4 blocks.
- Due to the simple logical structure and performing many computational and logical operations, this block can be used in multi-bit arithmetic and logic unit, which will be optimal compared to existing designs in terms of cell number, occupied area, latency and quantum cost.

Proposed reversible ALU scheme.

The proposal includes a novel BS1 Block, reversible Feynman gates, and Fredkin gates. The quantum form of the proposed ALU unit is shown in Figure 8. In the proposed design, C2 and C3 control the A and B inputs of the Feynman gates. A Feynman bidirectional gate is a logic gate that can be used to perform operations on either A or B, or their complements. If you need input A or B, set the control input of the preferred gate to zero, and if you need the corresponding input of input B, set the control input to one. For example, the second Feynman gate outputs Q if C2 = 0, and An if C2 = 1, which is then fed into the proposed building block. The proposed design has two outputs, O1 and O2, and the Fredkin gate is used to select between them. The control input of the Fredkin gate is linked to C1 in the proposed setup. The Fredkin conclusions are equal to having C1 = 0.

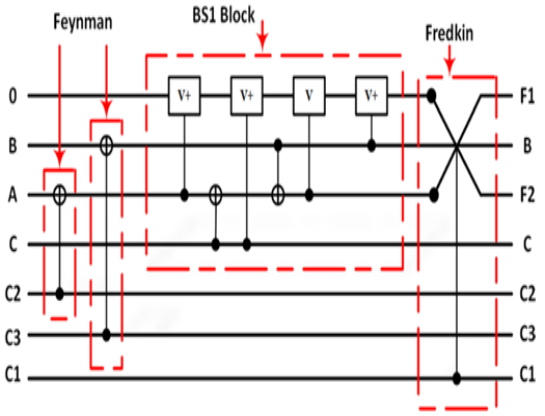


Fig. 8 Quantum structure of the proposed reversible ALU unit

If C1 = 1, the results are flipped from Q = B and R = C to Q = C and R = B. As an added bonus, the suggested BS1 Block can perform both logical and numeric calculations. This plan has a quantum cost of thirteen.

Logic and arithmetic operations of the proposed ALU unit

Twenty mathematical and logical functions are available in this system. The suggested architecture has six inputs labelled C1, C2, C3, A, B, and C and two outputs labelled F1 and F2. The data stream into this structure is dependable, and it produces no junk at all (two outputs B and C can be used as inputs in the next block). This structure can execute a wide variety of logical and mathematical operations, including AND, NOR, XOR, NAND, XNOR, OR, and transfer, reversing input, increase, borrowing (subtracting with borrowed number), and carrying. Table 1 displays all of the mathematical and logical processes that can be performed by the suggested system.

Simulation and comparison of results

To model the suggested architecture, this article makes use of the Codesigned 2.0.3 application. Quickly create, arrange, and simulate QCA circuits

ISSN: 1832-5505

Vol-10 Issue-04 OCT 2022

with the help of Codesigned software [5]. Simulation and performance findings for the proposed BS1 Block, the proposed ALU circuit, and a contrast and assessment of the proposed design in light of prior study are discussed below. Except for the amount of samples, which is set to 128,000 by default, all other modelling settings have present values.

Table 1 Proposed ALU logic and arithmetic operations

Control Inputs			Operands			Outputs		
C_1	C_2	C_3	A	B	C	F_1	F_2	
0	0	0	A	0	0	0	A	Arithmetic Operations
0	0	0	A	1	0	A	$\bar{A}$	
0	0	0	A	0	1	C_{out}	$A+1$	
0	0	0	A	B	C_i	C_{out}	$A+B$	
0	1	0	A	B	C_i	Brw	$A-B$	
0	1	1	A	B	1	Brw	B − A	
0	1	0	A	B	0	$A\bar{B}$	$\bar{A}\oplus B$	Logic Operations
0	1	1	A	B	0	$\bar{A}\,\bar{B}$	$\bar{A}\oplus\bar{B}$	
1	0	0	A	B	0	$A\oplus B$	AB	
1	0	0	A	B	1	$A\odot B$	$A+B$	
1	0	1	A	B	0	$A\oplus\bar{B}$	$A\,\bar{B}$	
1	0	1	A	B	1	$A\oplus B$	$A+\bar{B}$	
1	1	0	A	B	0	$\bar{A}\oplus B$	$\bar{A}B$	
1	1	0	A	B	1	$\bar{A}\oplus\bar{B}$	$\bar{A}+B$	
1	1	1	A	B	0	$\bar{A}\oplus\bar{B}$	$\overline{A+B}$	
1	1	1	A	B	1	$A\odot B$	$\overline{AB}$	

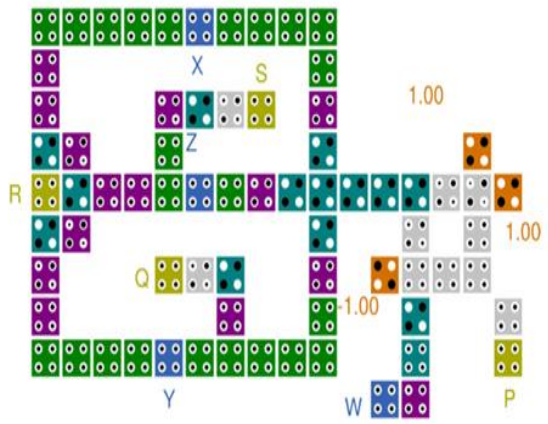


Fig. 9 BS1 Block simulation by QCA cells

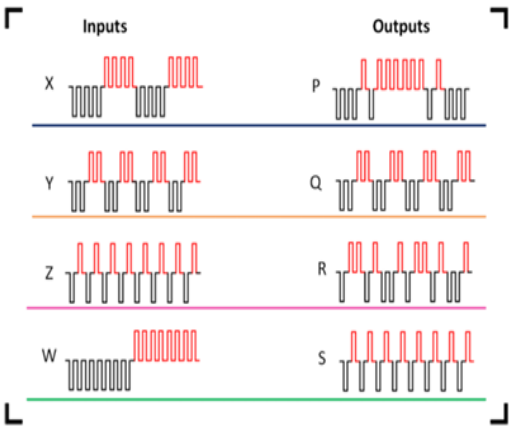


Fig. 10 the simulation result of BS1 Block

Proposed reversible block simulation BS1 block.

In Fig. 9, we can see the results of the suggested QCA-based modelling of the BS1 Block. Inputs (W, X, Y, and Z) lead to products (P, Q, R, and S). This section constitutes the bulk of the planned ALU. The suggested BS1 Block wasmodelled with the help of two XOR gates and a consensus user. 72 cells with diameters of 18 nanometre, area of 0.08 m2, and a delay of 3 stages' clock cycles were used to model the block. Similarly, Fig. 10 displays the simulation's outcome. It can be seen from Fig. 10 that the values P = 1, Q = 1, R = 0, and S = 1 result from the inputs W = 0, X = 0, Y = 1, and Z = 1. The values P, Q, R, and S are produced when the inputs W, X, Y, and Z are all 1.

Proposed reversible ALU simulation.

Figure 11 shows the results of a test of the suggested QCA-based bidirectional ALU. The architecture consists of a Fredkin gate, two Feynman gates, and the suggested bidirectional BS1 Block for conducting logic and math functions. The suggested ALU relies heavily on the BS1 Code. The BS1 Block takes in signals at A, B, C, and S. In the suggested design, S equals zero, A, B, and C are set from the outputs of the two Feynman gates, and D is a constant. All of these numbers are taken from Table 1. The P and R outputs of BS1 Block serve as Fredkin inputs, which are used as multiplexers in the ALU architecture to define the necessary processes and decide the end output. The suggested ALU exercise is based on QCA and is carried out on a 0.52 m2 region with 350 cells operating in 3 different clock

ISSN: 1832-5505

Vol-10 Issue-04 OCT 2022

pulse zones. Figure 12 depicts the outcome of a modelling of the circuit.

Evaluation and comparison

The suggested ALU is compared to other works in this field in terms of metrics like number of processes, delay, quantum cost, number of cells, and area taken up. The ALUs suggested in [24, 28] will be evaluated in QCA-based experiments in terms of cell density and surface area occupancy to determine which is superior. When compared to planned ALUs, the suggested ALU has many more cells, making it more efficient. When compared to these ALUs, it also performs better in terms of delay and space utilization. Table 2 provides an overview of the differences made between the provided ALUs and the ALUs generated using QCA. Compared to [24, 28], Fig. 13 displays the suggested method's increase in percentage form. When compared to the approaches in [24] and [28], the suggested ALU improves the filled area measure by 45% and 30%, respectively.

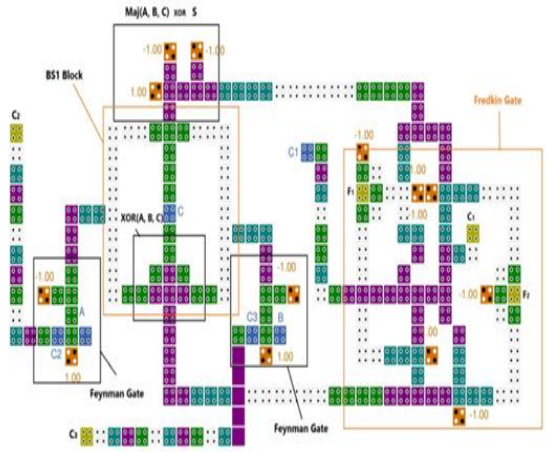
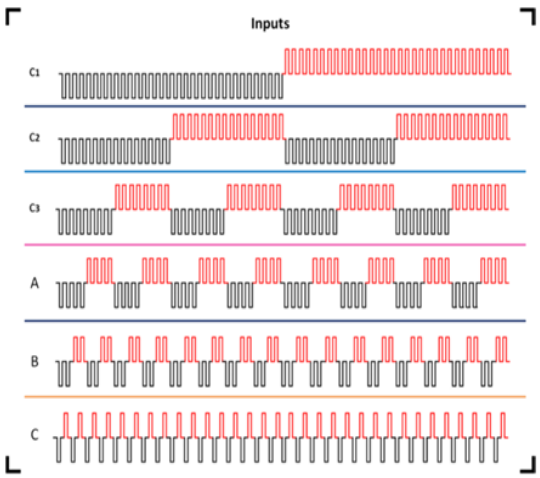


Fig. 11 Simulation of an ALU unit designed using QCA cells



(a)

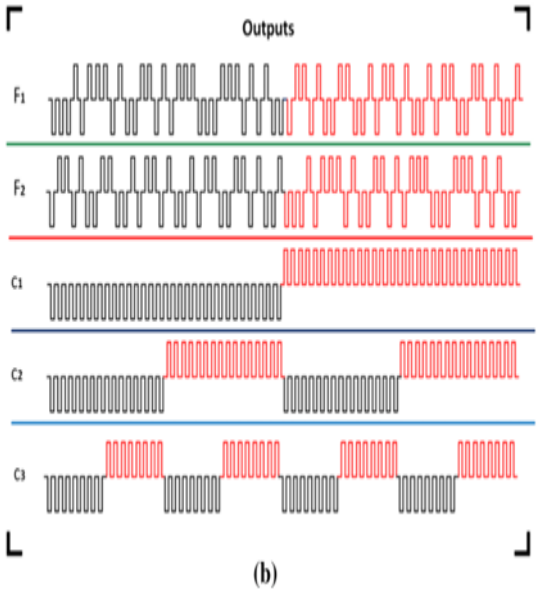


Fig. 12 Simulation result; a inputs and b outputs

Conclusion and future work:

In this work, we introduce a reversible ALU that consists of a four-by-four reversible block (the BS1 Block), a three-by-three reversible Fredkin gate, and two two-by-two Feynman gates. The suggested BS1 Block is a reversible 44 block with a quantum cost of 6.

Table 2 Comparison of ALU presented with previous researches.

Ref.	Operations	Quantum cost	Latency	Number of cells	Area (μm^2)
[24]	16	21	16	670	0.921
[23]	4	14	16	464	0.78
[22]	21	18	12	1069	2.34
[27]	4	13	12	332	0.38
[28]	20	20	15	480	0.75
Proposed	20	13	12	350	0.52

ISSN: 1832-5505

Vol-10 Issue-04 OCT 2022

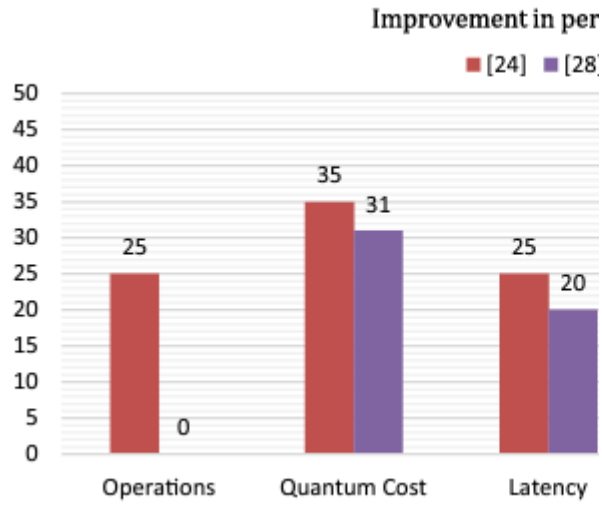


Fig. 13 Improvement in percentage of the proposed method compared to previous studies.

There are two XOR gates and one three-input consensus built into the design of the BS1 Block. Benefits of the suggested bidirectional ALU include reduced quantum cost, cell count, delay, and floor space requirements. The suggested plans are simulated with the help of the Codesigned 2.0.3 program. QCA technology is used for simulation of the suggested bidirectional ALU. The suggested layout consists of 250 units and occupies 0.30 m2. When it comes to assessment metrics like cell count, delay, and filled area, our QCA-designed bidirectional ALU outperforms the state-of-the-art. Reduce the number of cells, the quantum cost, the number of processes, and the delay by using novel forms of logical reversible gates like XOR in the future.

References

1. Landauer R (1961) Irreversibility and heat generation in the computational process. IBM J Res Dev 5:183–191
2. Bennett C (1973) Logical reversibility of computation. IBM J Res Dev 17:525–532
3. Das JC, De D (2019) Novel design of reversible priority encoder in quantum dot cellular automata based on Toffoli gate and Feynman gate. J Supercomputer 75:6882–6903
4. Sasami TN, Singh AK, Mohan A (2016) Efficient design of reversible Alu in quantum-dot cellular automata. Optic, p 6172–6182
5. Das JC, De D (2015) Novel low power reversible binary incremented design using quantum-dot cellular automata. Microprocess Microcyst 42:10–23
6. Sousa L (2021) Nonconventional computer arithmetic circuits, systems, and applications. IEEE CircaSits Mag 21:6–40
7. Bishop D (2005) Nanotechnology and the end of Moore's law. Bell Labs Tech J 10:23–28
8. Roohi A, DeMara R, Khichadi N (2015) Design and evaluation of an ultra-area-efficient fault-tolerant QCA full adder. J Microelectron 46:531–542
9. Sabbaghi-Nadooshan R, Kianpour M (2014) A novel QCA implementation of MUX-based universal shift register. Computer Electron
10. Mohar rami E, Jafari Azimpour N (2017) Designing nanoscale counter using reversible gate based on quantum-dot cellular automata. Int J Theor Phys, pp 1060–1081
11. Ahmad F, Bhat G (2012) Novel code converters based on quantum-dot cellular automata (QCA). Journal of Science and Research, p. 364–371, 2012.
12. M. Sarvashay-Moghaddam, Srouji AA (2018) A new design and simulation of reversible gates in quantum-dot cellular automata technology
13. Walus K, Dysart T, Jullien G, Budiman R (2004) Codesigned: a rapid design and simulation tool for quantum-dot cellular automata. IEEE Trans Nanotechnology 3(1):26–31
14. Bahar A, Rahman M, Nahid N, Hassan M (2017) Energy dissipation dataset for reversible logic gates in quantum dot-cellular automata. Data Brief 10:557–560
15. Bah repour D, Farzana J (2016) A novel robust microcell based on quantum dot cellular automata. Quantum Matter 5:689–696